



EFC6602R

N-Channel Power MOSFET 12V, 18A, 5.9mΩ, Dual EFCP

ON Semiconductor®

<http://onsemi.com>

Features

- 2.5V drive
- Common-drain type
- 2KV ESD HBM
- Protection diode in
- Halogen free compliance

Specifications

Absolute Maximum Ratings at Ta=25°C

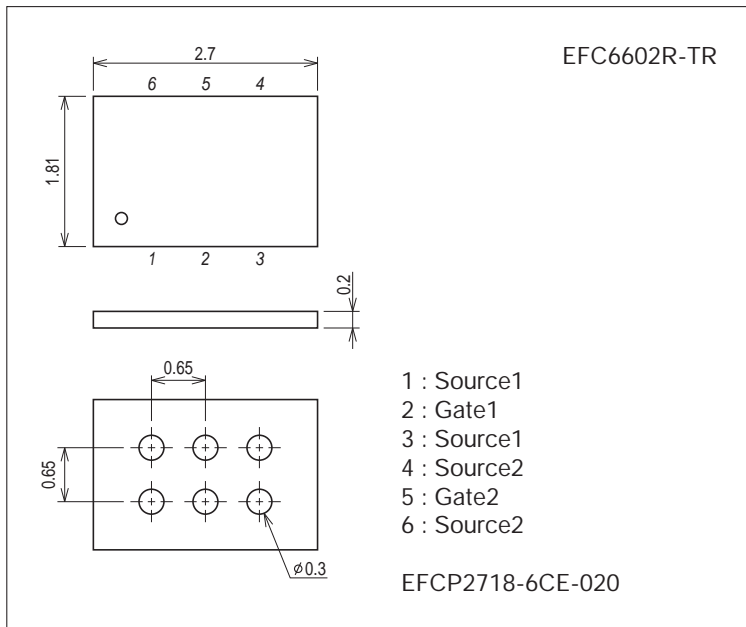
Parameter	Symbol	Conditions	Ratings	Unit
Source-to-Source Voltage	V _{SSS}		12	V
Gate-to-Source Voltage	V _{GSS}		±12	V
Source Current (DC)	I _S		18	A
Source Current (Pulse)	I _{SP}	PW≤10μs, duty cycle≤1%	60	A
Total Dissipation	P _T	When mounted on ceramic substrate (5000mm²×0.8mm)	2.0	W
Channel Temperature	T _{ch}		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

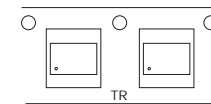
7073-001



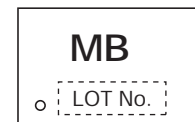
Product & Package Information

- Package : EFCP
- JEITA, JEDEC : -
- Minimum Packing Quantity : 5,000 pcs./reel

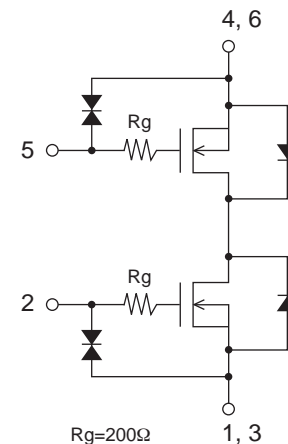
Taping Type : TR



Marking



Electrical Connection



EFC6602R

Electrical Characteristics at Ta=25°C

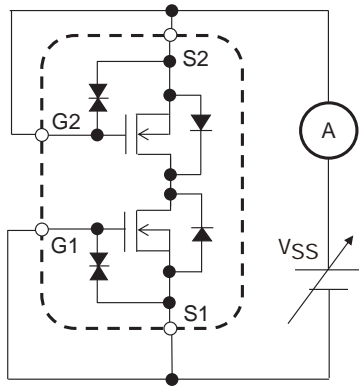
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Source-to-Source Breakdown Voltage	V(BR)SSS	IS=1mA, VGS=0V Test Circuit 1	12			V
Zero-Gate Voltage Source Current	ISSS	VSS=10V, VGS=0V Test Circuit 1			1	μA
Gate-to-Source Leakage Current	IGSS	VGS=±8V, VSS=0V Test Circuit 2			±1	μA
Cutoff Voltage	VGS(off)	VSS=6V, IS=1mA Test Circuit 3	0.5		1.3	V
Forward Transfer Admittance	yfs	VSS=6V, IS=3A Test Circuit 4		13		S
Static Source-to-Source On-State Resistance	RSS(on)1	IS=3A, VGS=4.5V Test Circuit 5	3.1	4.5	5.9	mΩ
	RSS(on)2	IS=3A, VGS=4.0V Test Circuit 5	3.3	4.8	6.3	mΩ
	RSS(on)3	IS=3A, VGS=3.8V Test Circuit 5	3.5	5	6.5	mΩ
	RSS(on)4	IS=3A, VGS=3.1V Test Circuit 5	4.0	5.8	8.2	mΩ
	RSS(on)5	IS=3A, VGS=2.5V Test Circuit 5	5.2	7.5	11	mΩ
Turn-ON Delay Time	td(on)	VDD=6V, VGS=4.5V, IS=3A Test Circuit 7		530		ns
Rise Time	tr			2100		ns
Turn-OFF Delay Time	td(off)			6200		ns
Fall Time	tf			5500		ns
Total Gate Charge	Qg		VDD=6V, VGS=4.5V, IS=18A Test Circuit 8		55	
Forward Source-to-Source Voltage	VF(S-S)	IS=3A, VGS=0V Test Circuit 6		0.76	1.2	V

Ordering Information

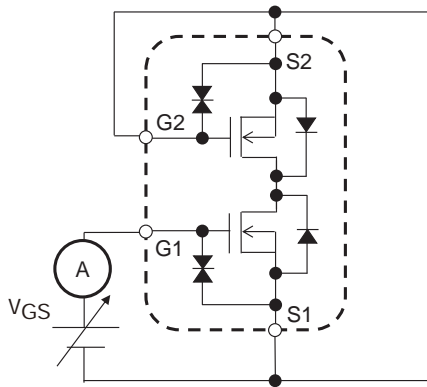
Device	Package	Shipping	memo
EFC6602R-TR	EFCP	5,000pcs./reel	Pb Free and Halogen Free

Test circuits are example of measuring FET1 side

Test Circuit 1
ISSS

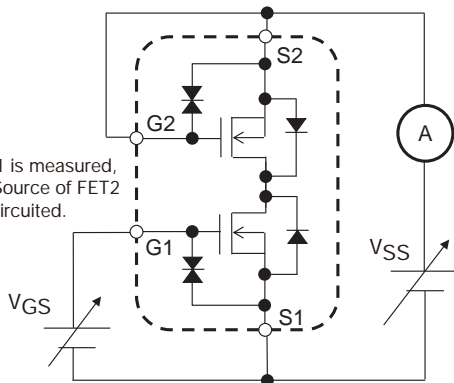


Test Circuit 2
IGSS



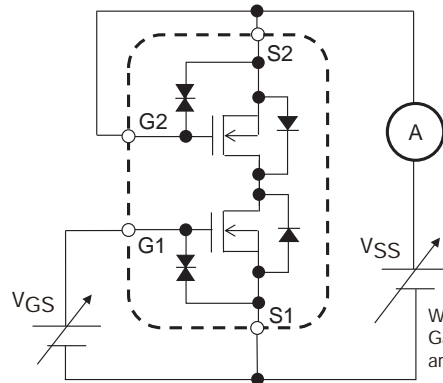
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
VGS(off)



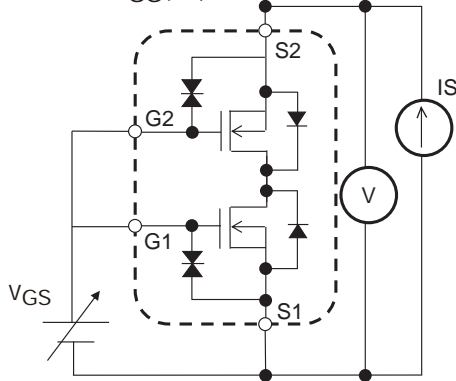
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
 $|y_{fs}|$

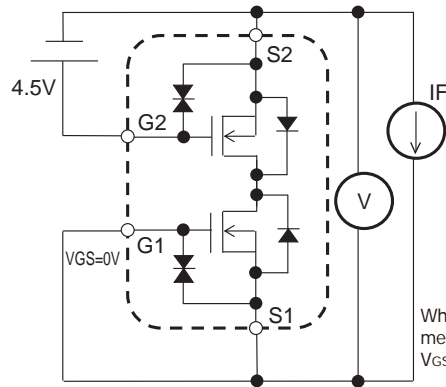


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 5
RSS(on)

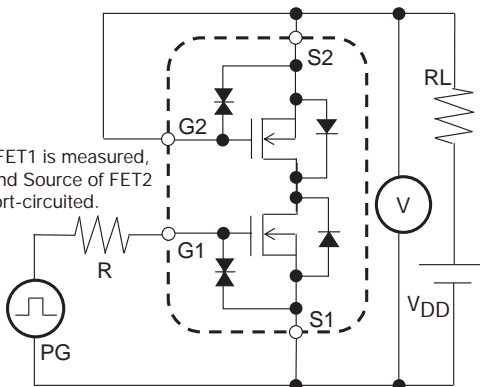


Test Circuit 6
VF(S-S)



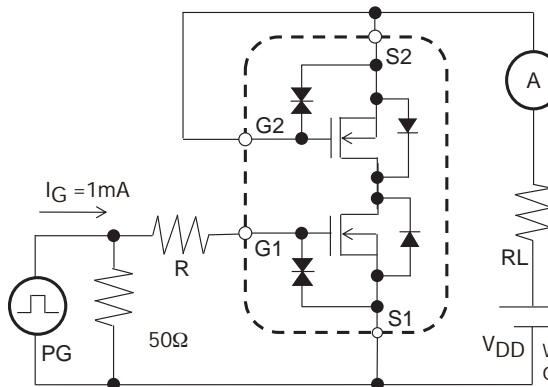
When FET1 is measured, +4.5V is added to Vgs of FET2.

Test Circuit 7
 $t_d(on)$, t_r , $t_d(off)$, t_f

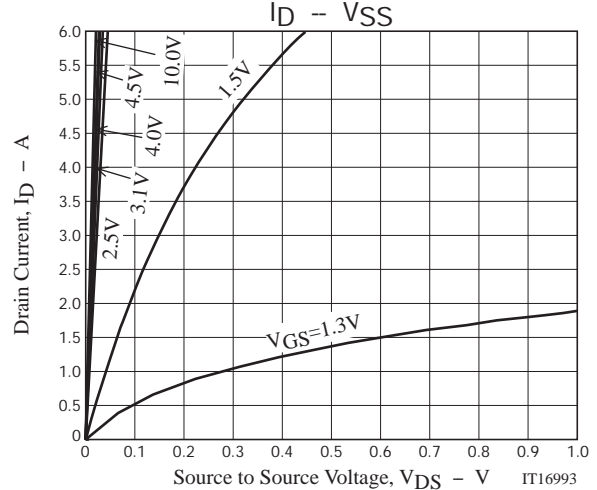
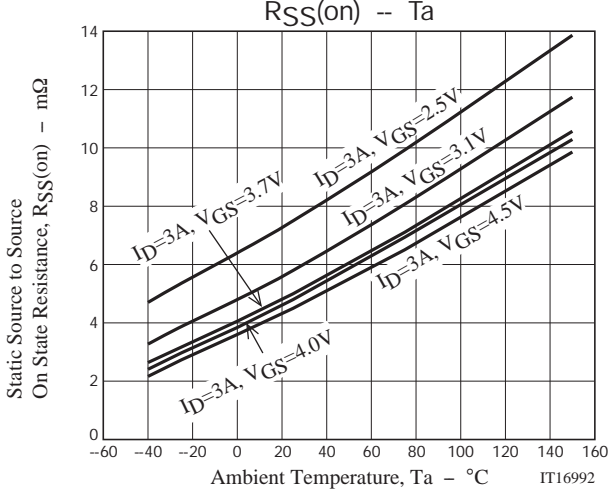
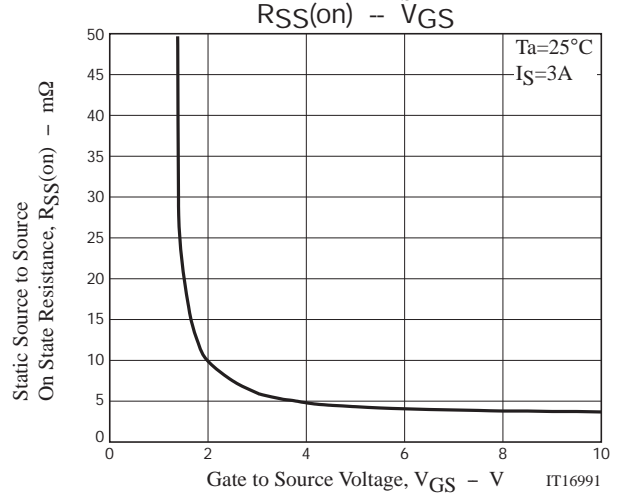
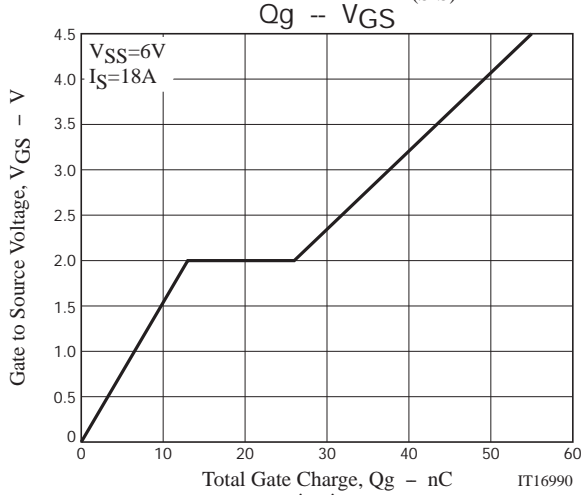
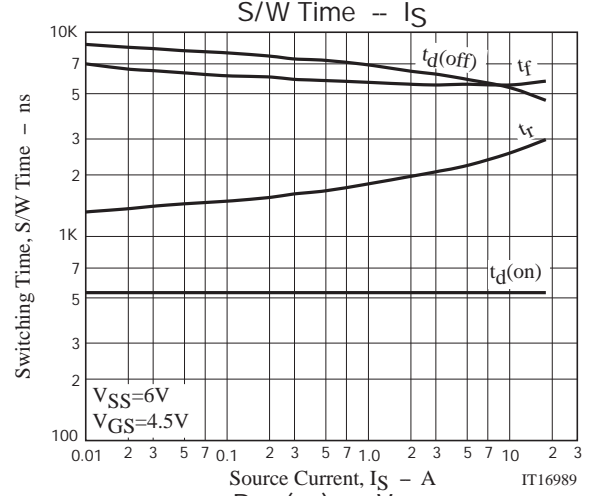
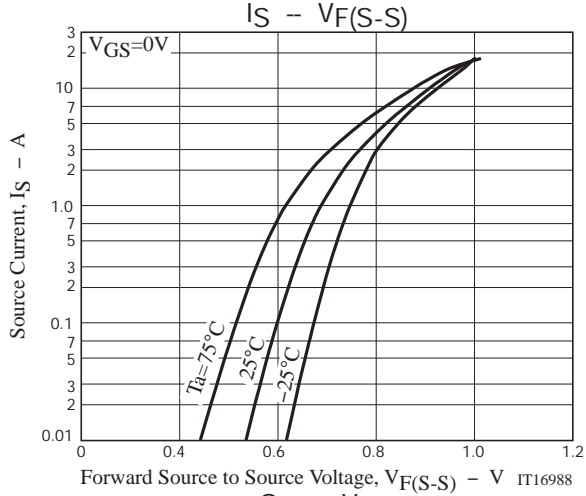
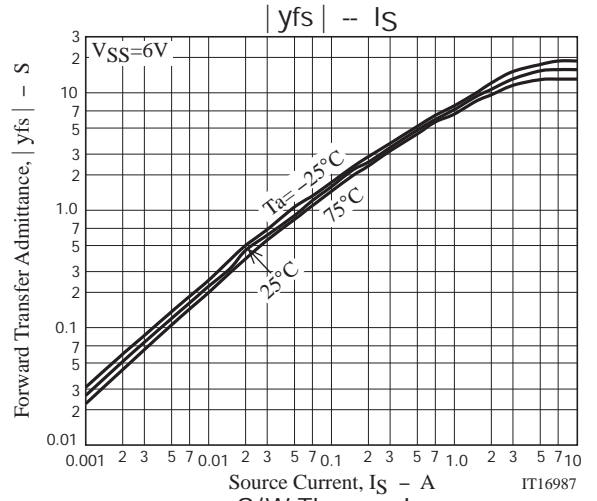
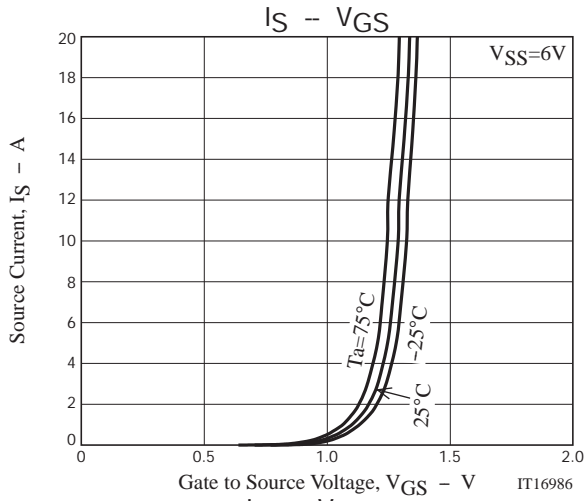


When FET1 is measured, Gate and Source of FET2 are short-circuited.

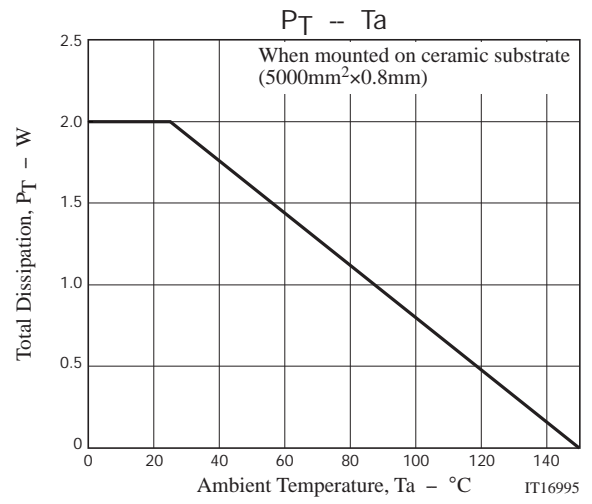
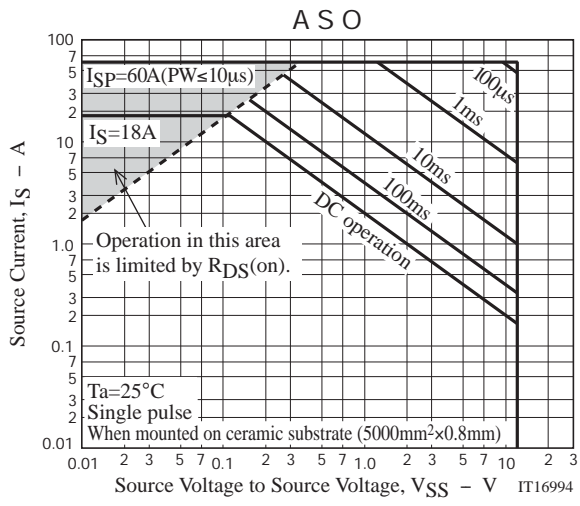
Test Circuit 8
Qg



When FET1 is measured, Gate and Source of FET2 are short-circuited.



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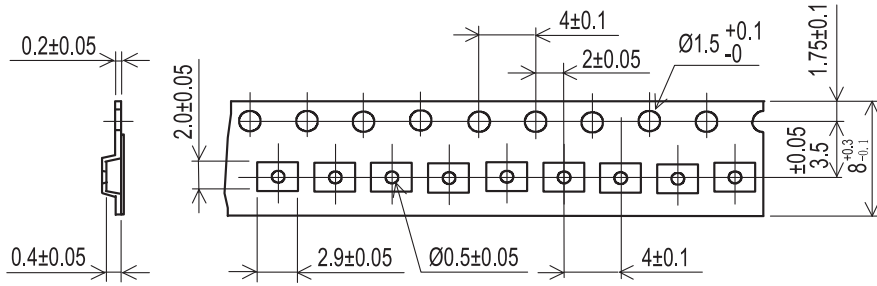


Taping Specification

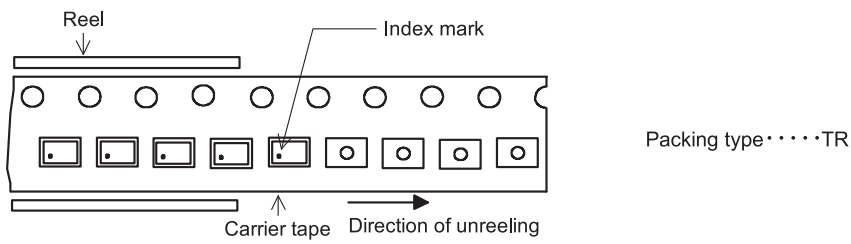
EFC6602R-TR

1. Taping Configuration

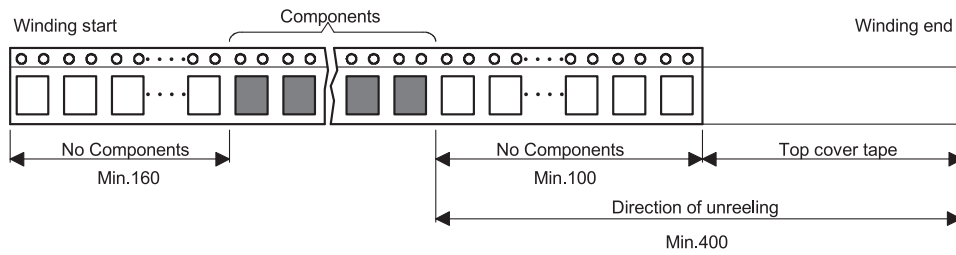
1-1 .Carrier Tape Size (unit:mm)



1-2 .Device Placement Direction



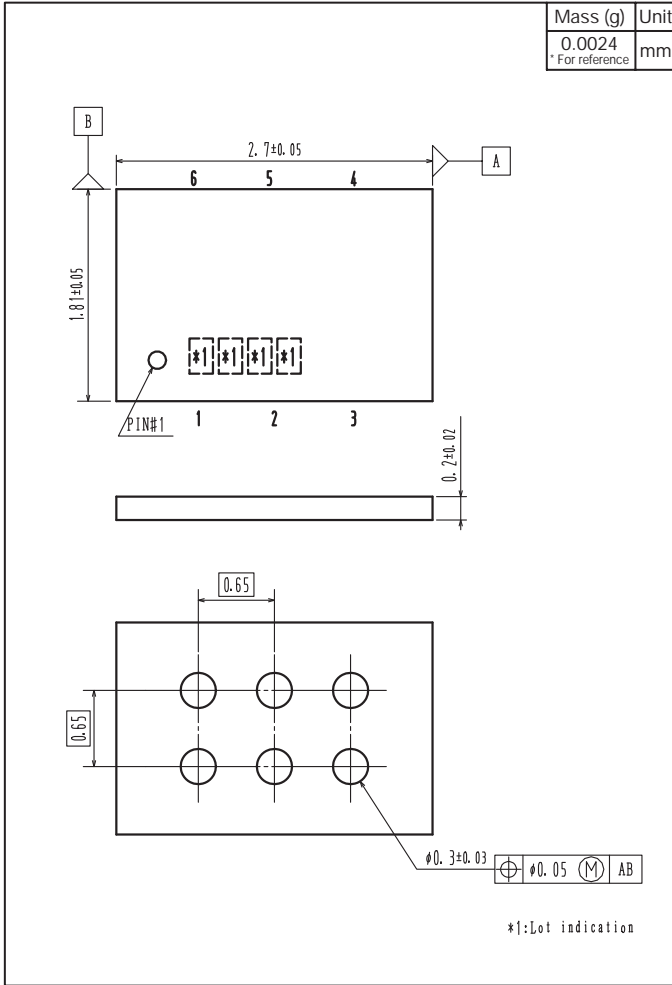
1-3 .Leader portion and Trailer portion (unit:mm)



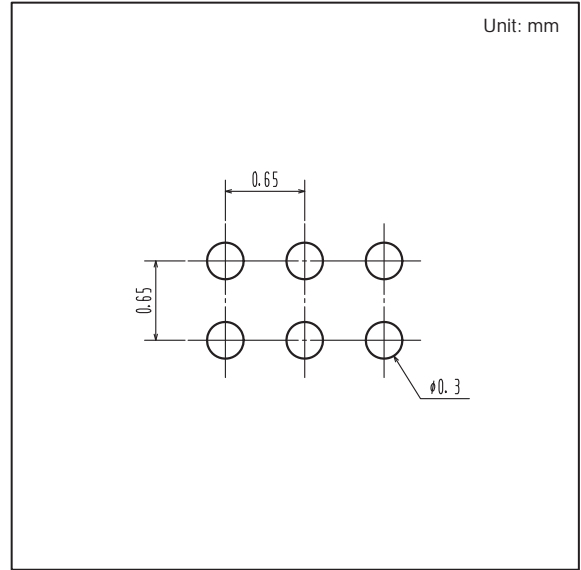
EFC6602R

Outline Drawing

EFC6602R-TR



Land Pattern Example



Note on usage : Since the EFC6602R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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